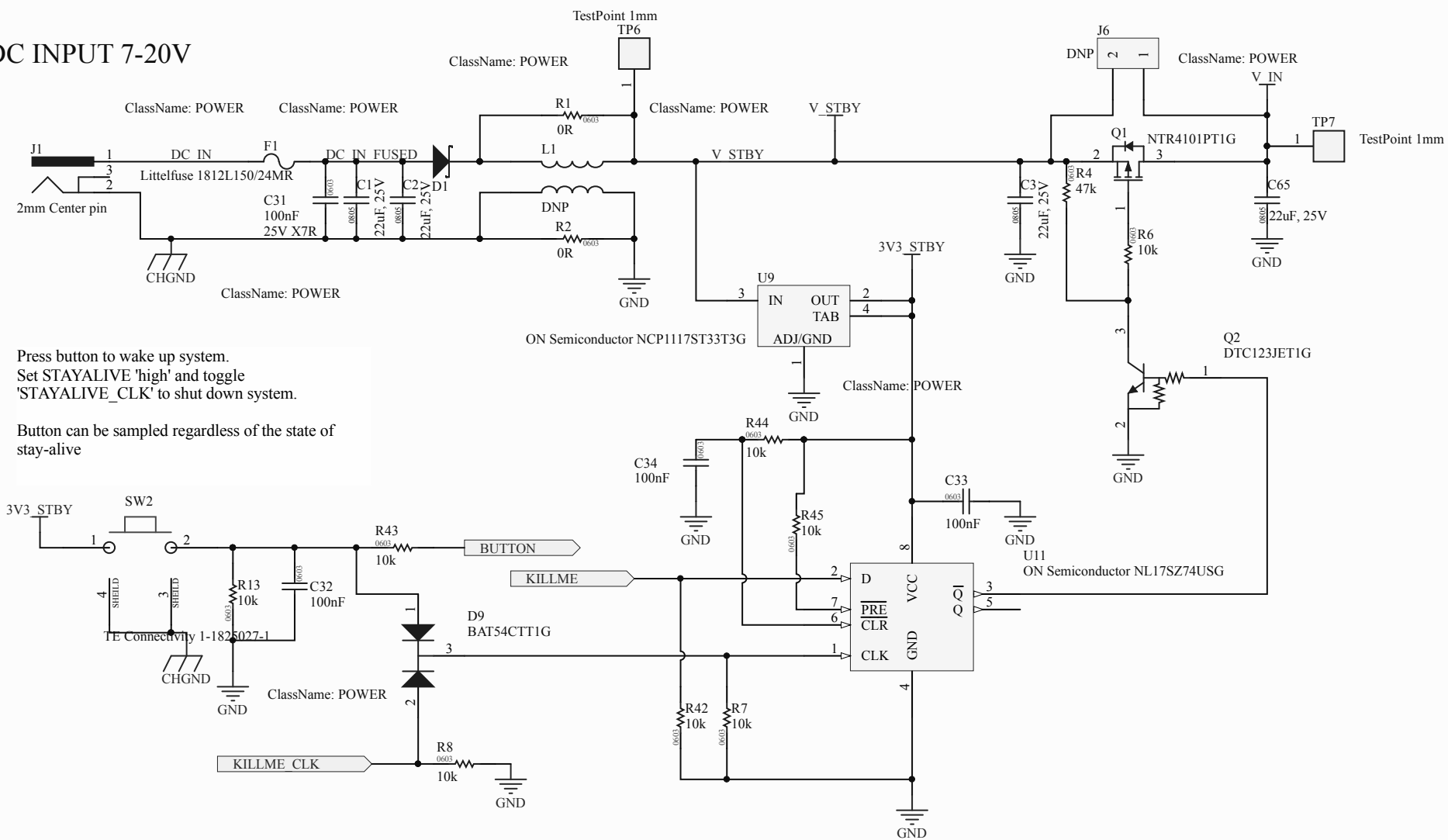
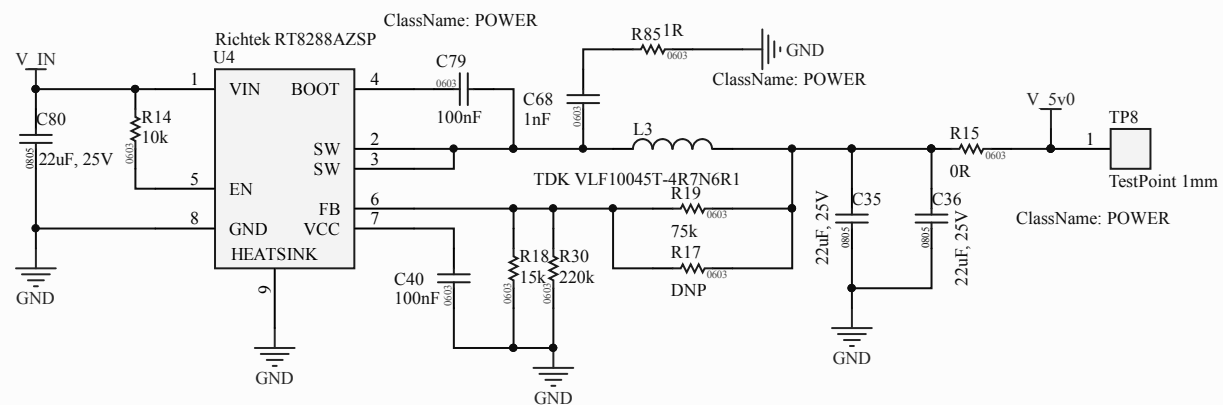


DC INPUT 7-20V



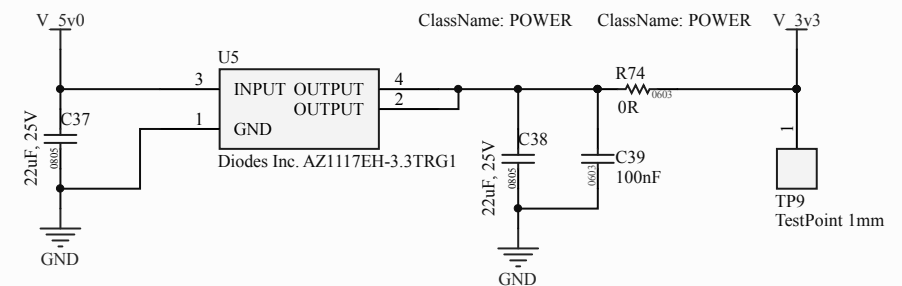
DC-DC Step Down, 5V 4A



Power budget

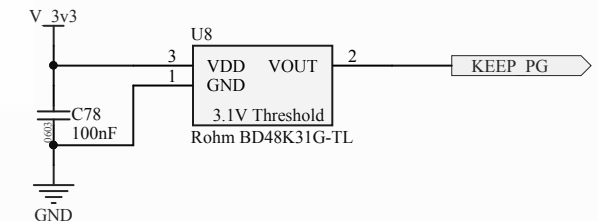
SoM 3.3V: 0.75W => 230mA (linear)
 SoM 5V: 7.5W => 1.5A
 2x SATA: 2x0.6A => 1.2A
 1x USB3: => 1A

Linear Regulator, 5V -> 3.3V



Power budget

SoM: 0.75W => 230mA
 eMMC: xx mA
 SATA: Probably 0
 PCIe: Allow for 500mA

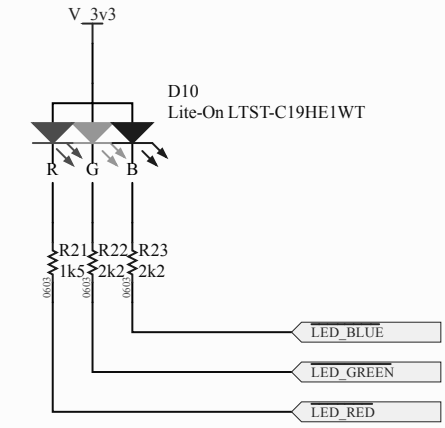
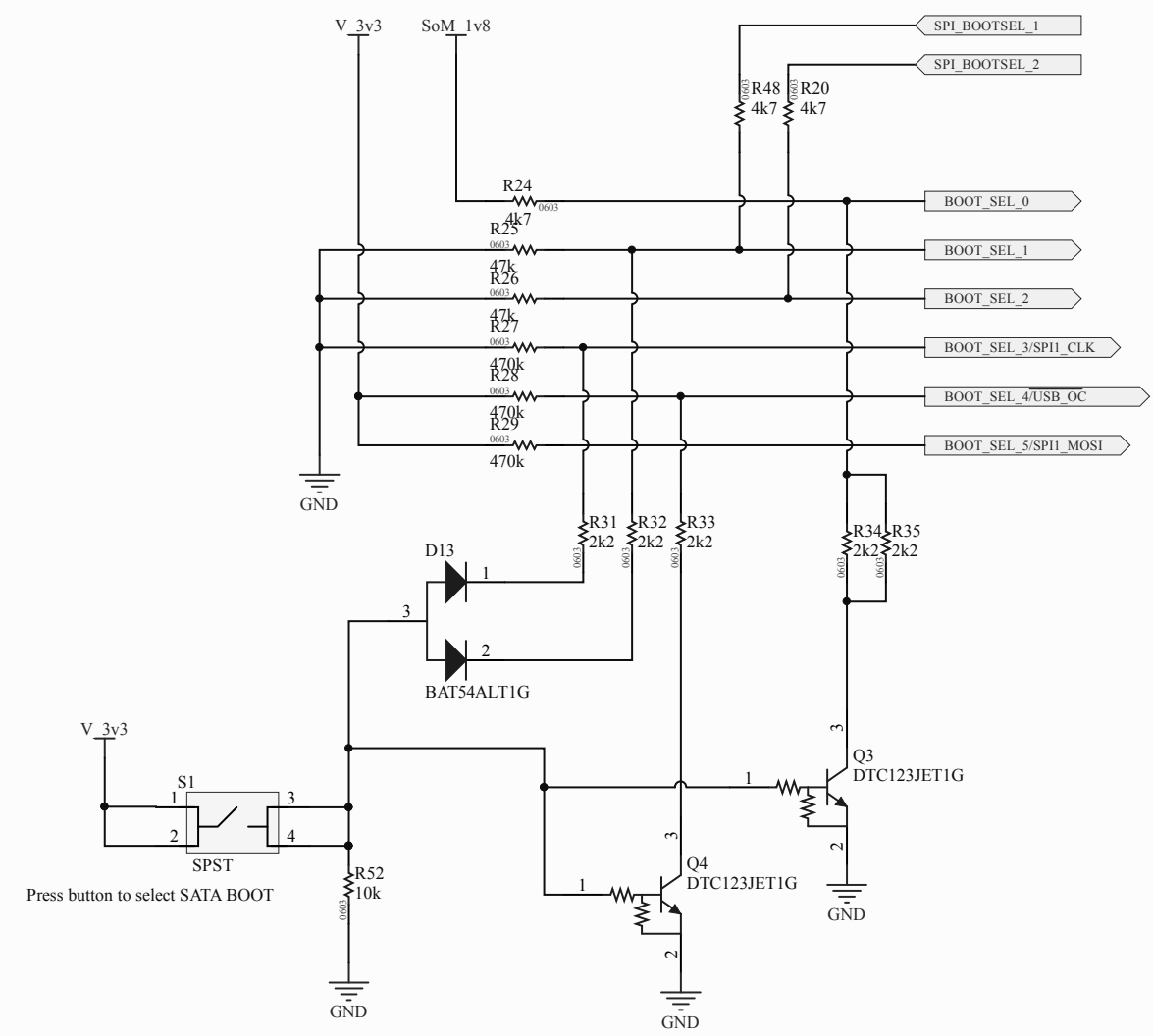


Title KEEP Base		OpenProducts Barsebäcksvägen 27 246 30 Löddeköpinge Sweden	
Size: A3	Revision: R1B	556855-1344	
Date: 2018-01-19	Time: 08:48:43	Sheet 1 of 1	
File: Power.SchDoc			

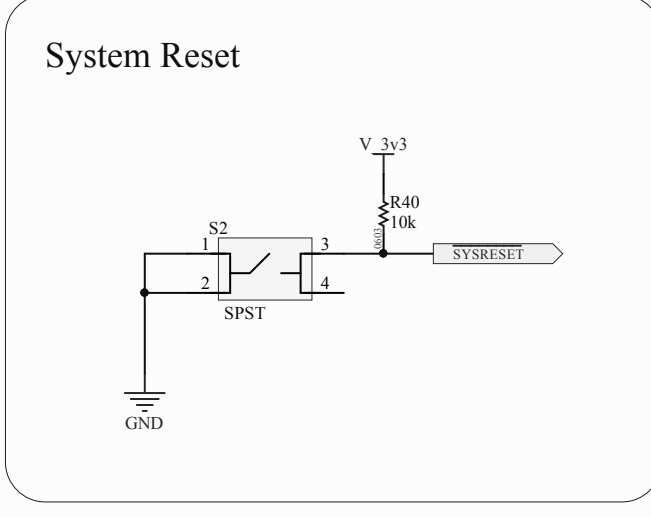
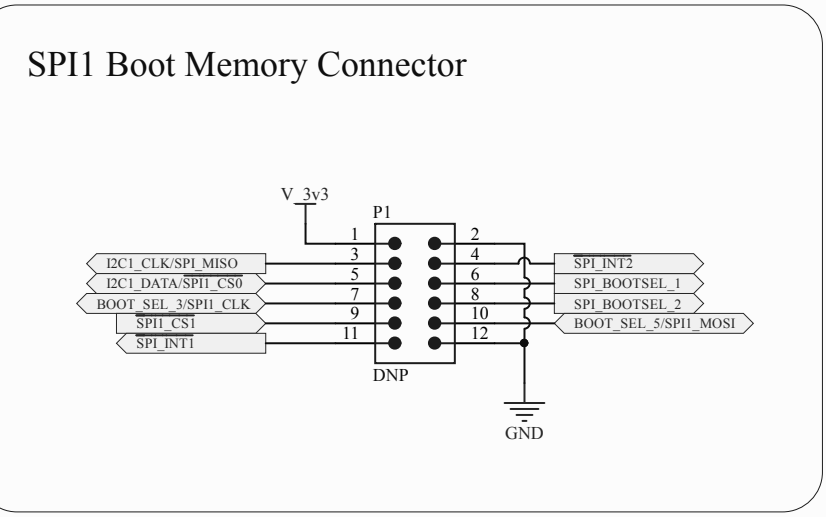
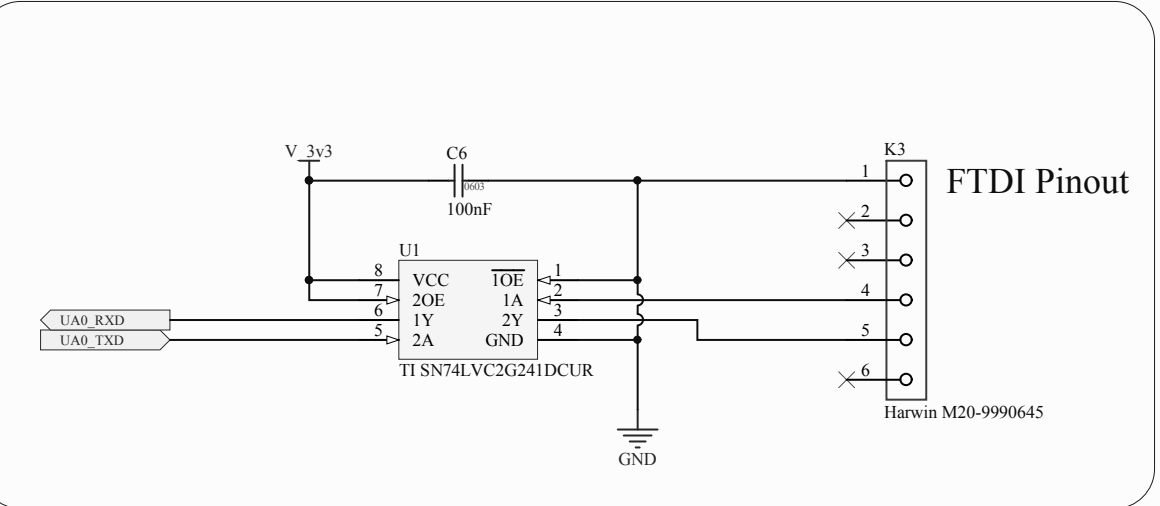
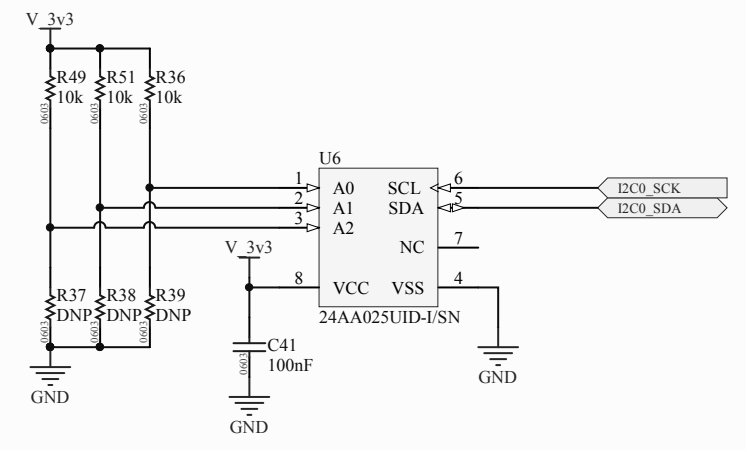
BOOT DEVICE SELECTION:

0x31: SDIO on MPP[40:37],MPP[28:24],MPP[21] (Default)
 0x2A: SATA SERDES0
 0x27: SPI1, MPP56-MPP59

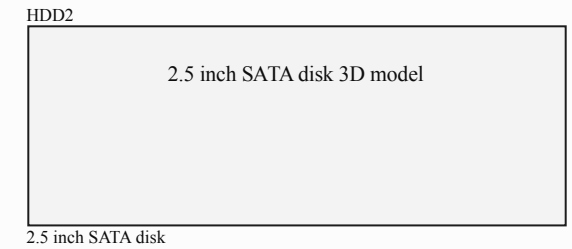
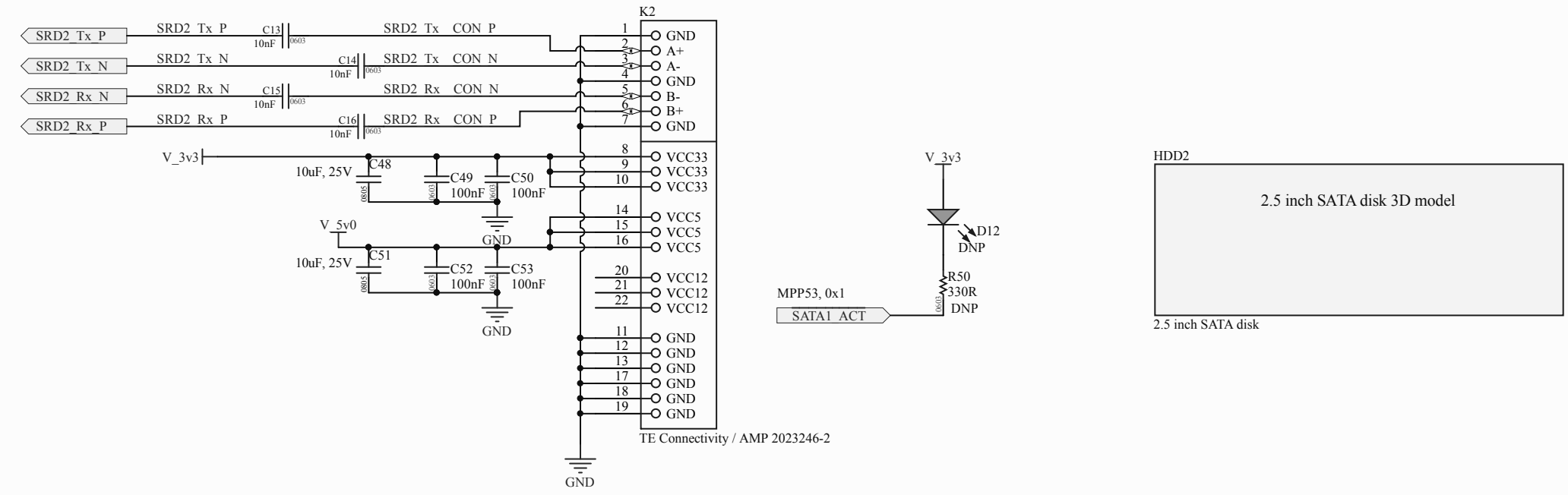
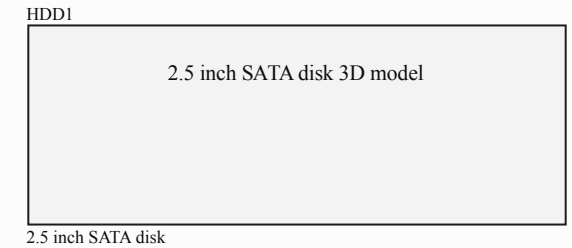
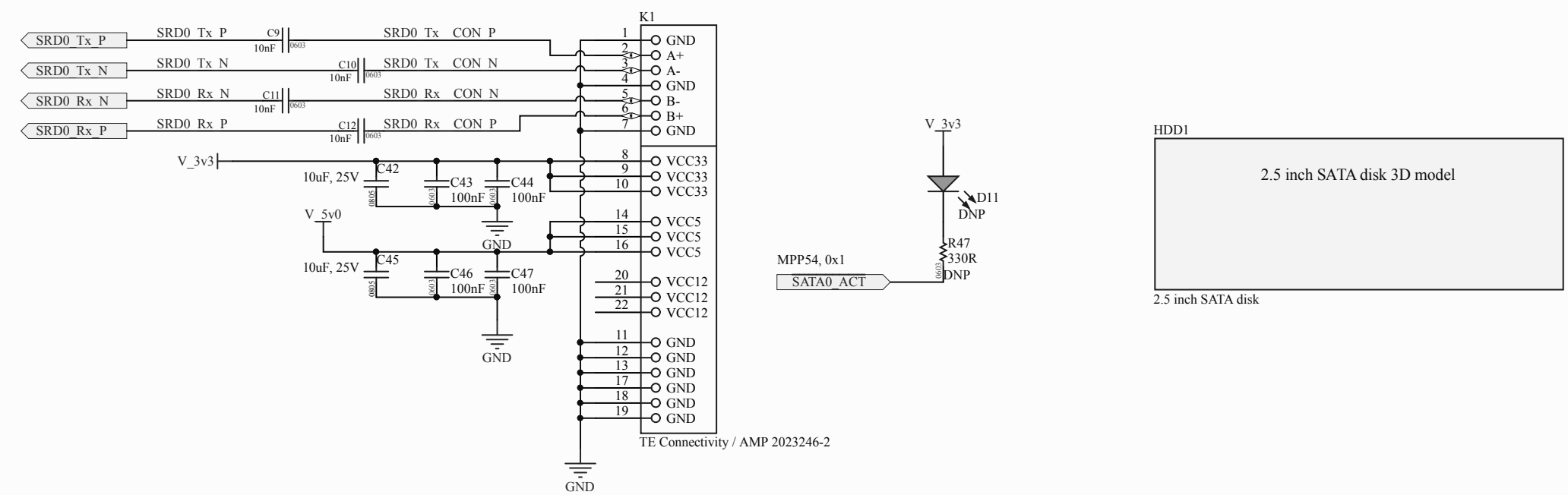
If no valid header is found, the device will try to boot from UART0



I2C Flash

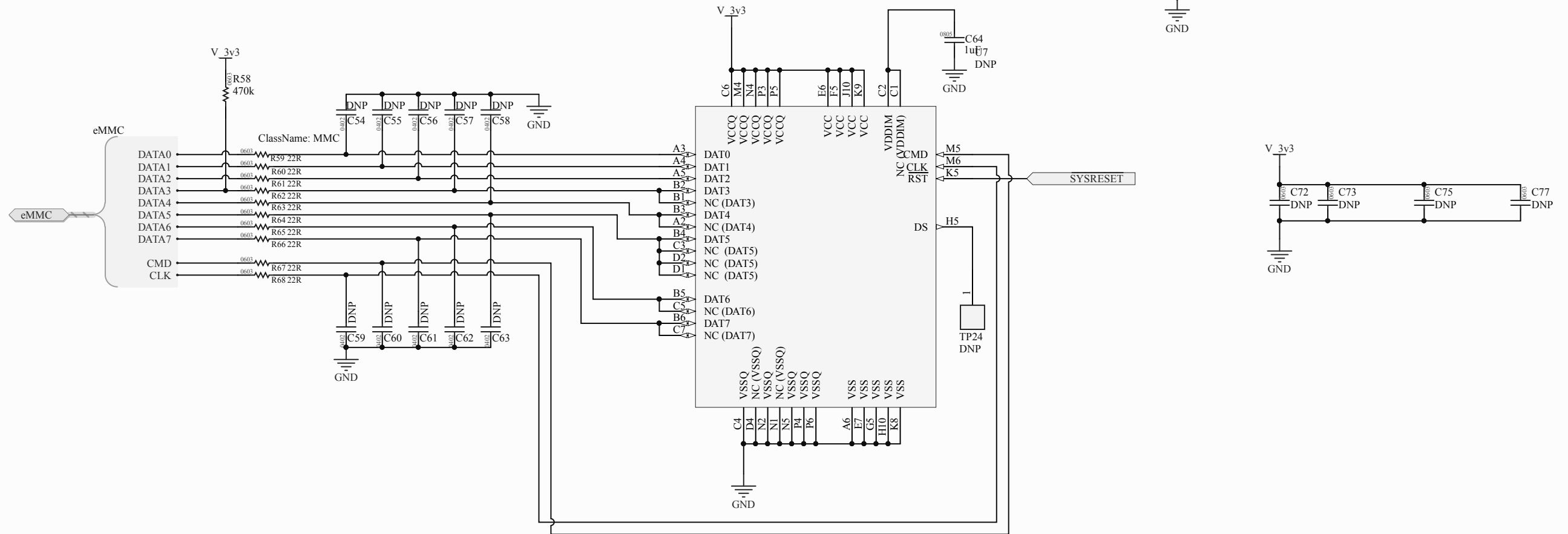


Title	KEEP Base	OpenProducts	Barsebäcksvägen 27 246 30 Löddeköpinge Sweden 556855-1344		
Size:	A3	Revision:			R1B
Date:	2018-01-19	Time:			08:48:43
File:	Connectors.SchDoc	Sheet* of *			

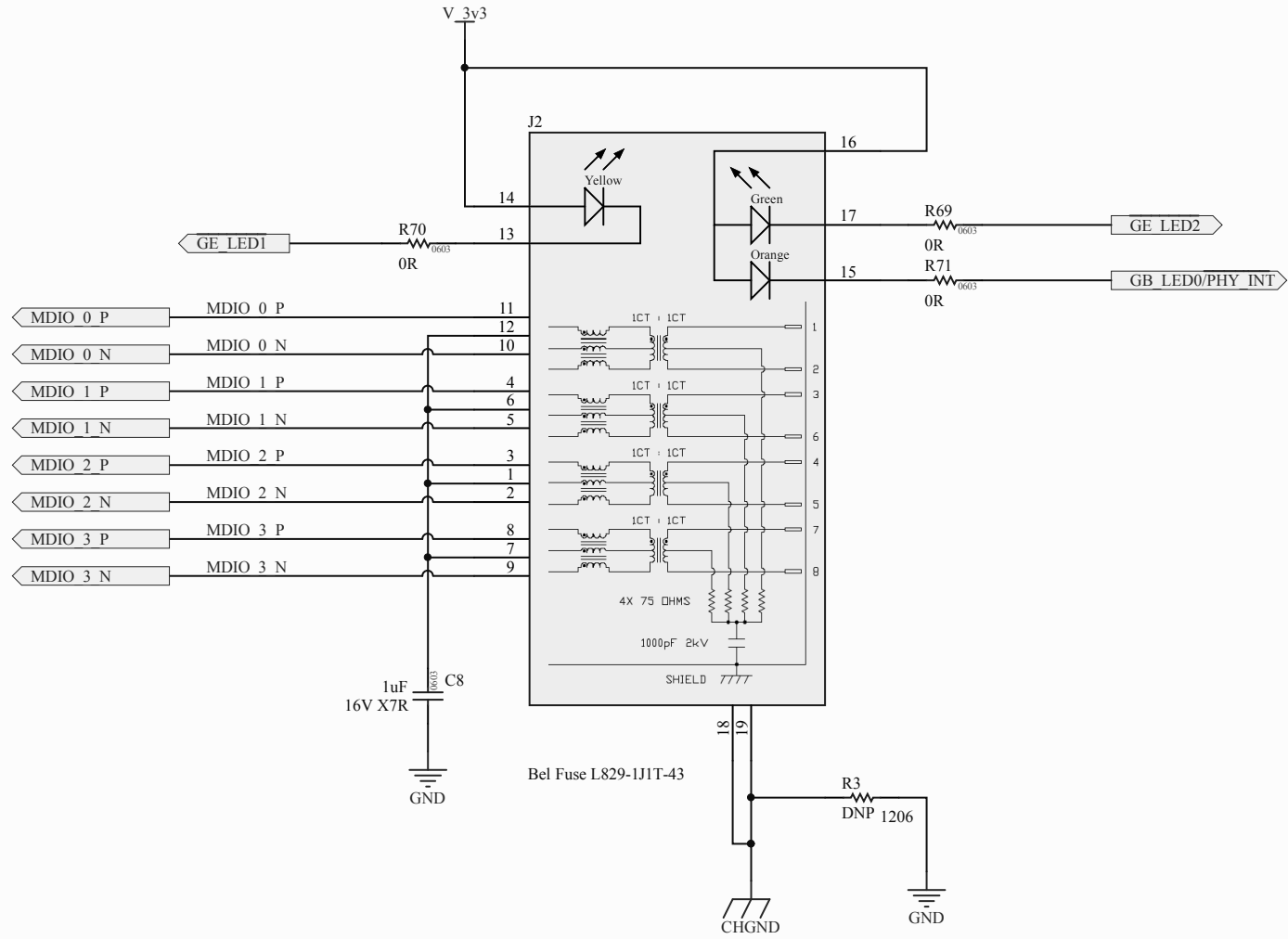


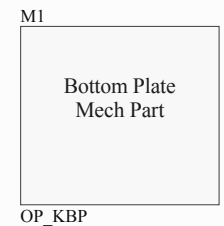
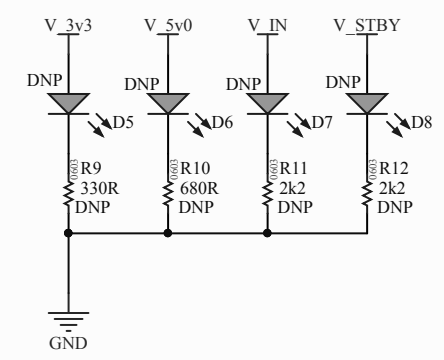
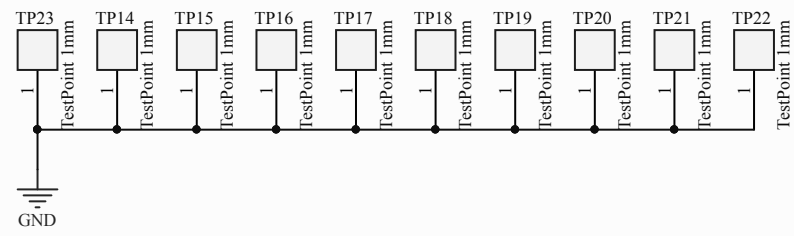
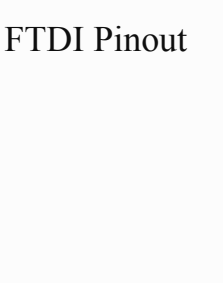
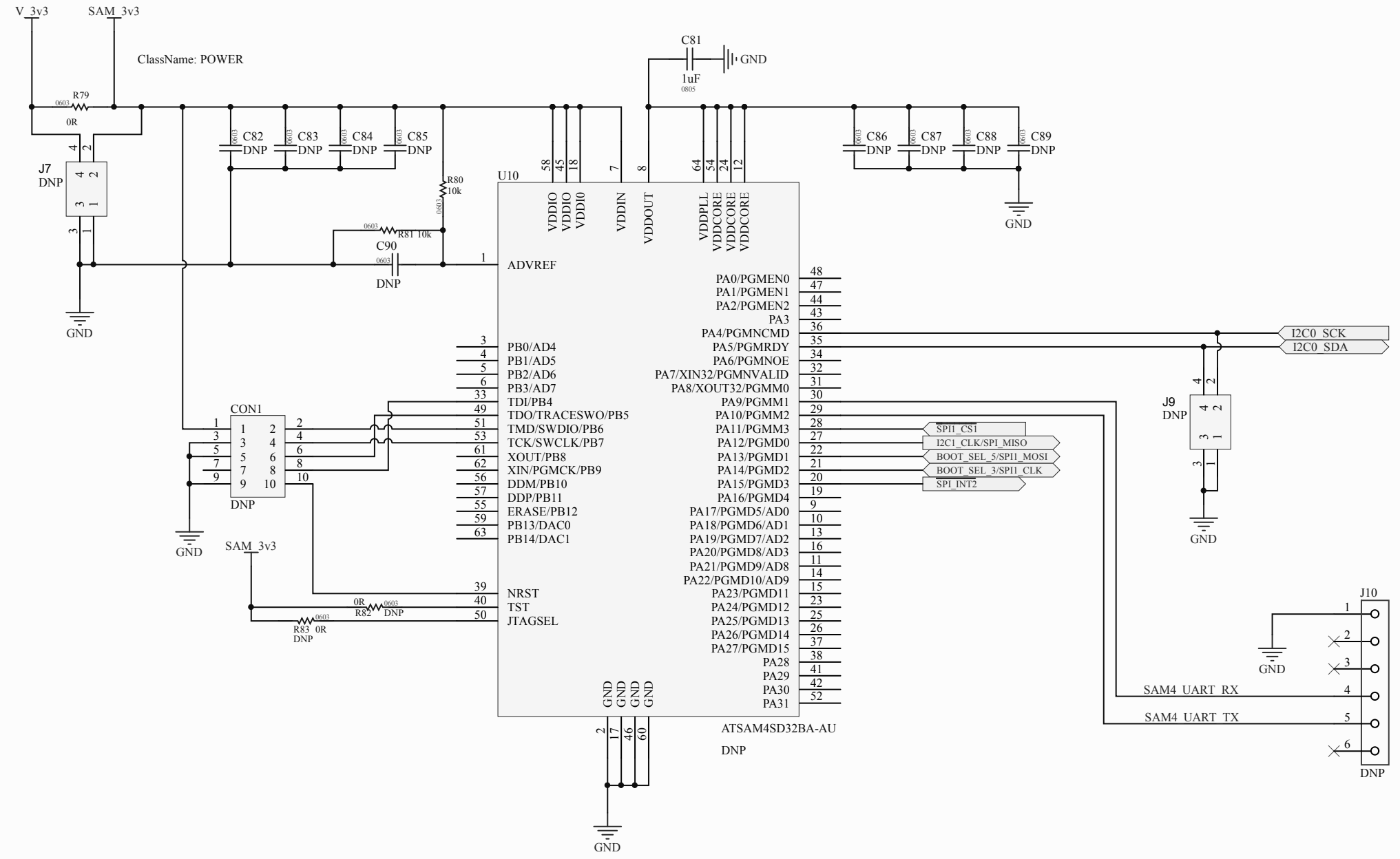
Title KEEP Base		OpenProducts Barsebäcksvägen 27 246 30 Löddeköpinge Sweden	
Size: A3	Revision: R1B	556855-1344	
Date: 2018-01-19	Time: 08:48:43	Sheet* of *	
File: disks.SchDoc			

eMMC components not placed



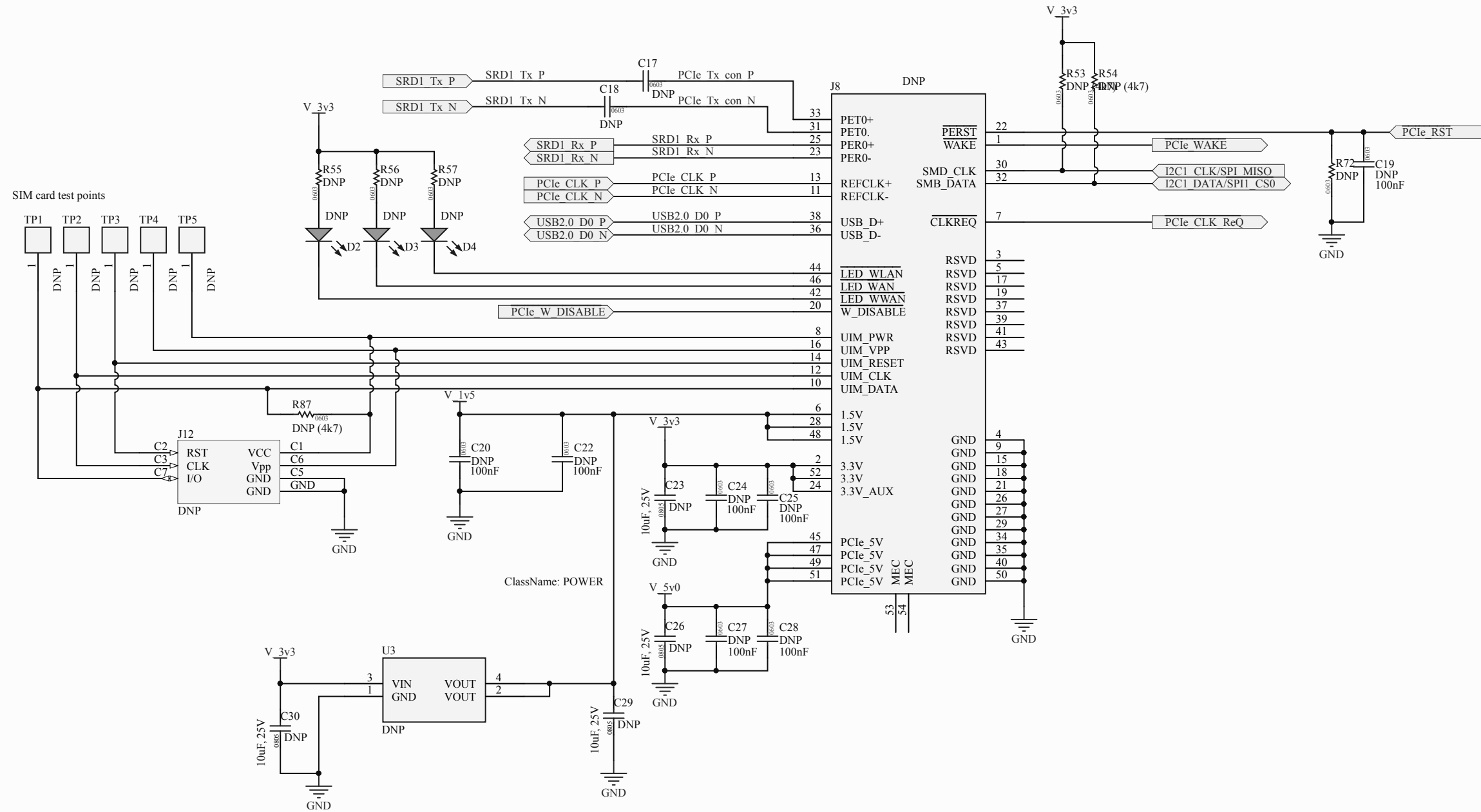
Gigabit Ethernet





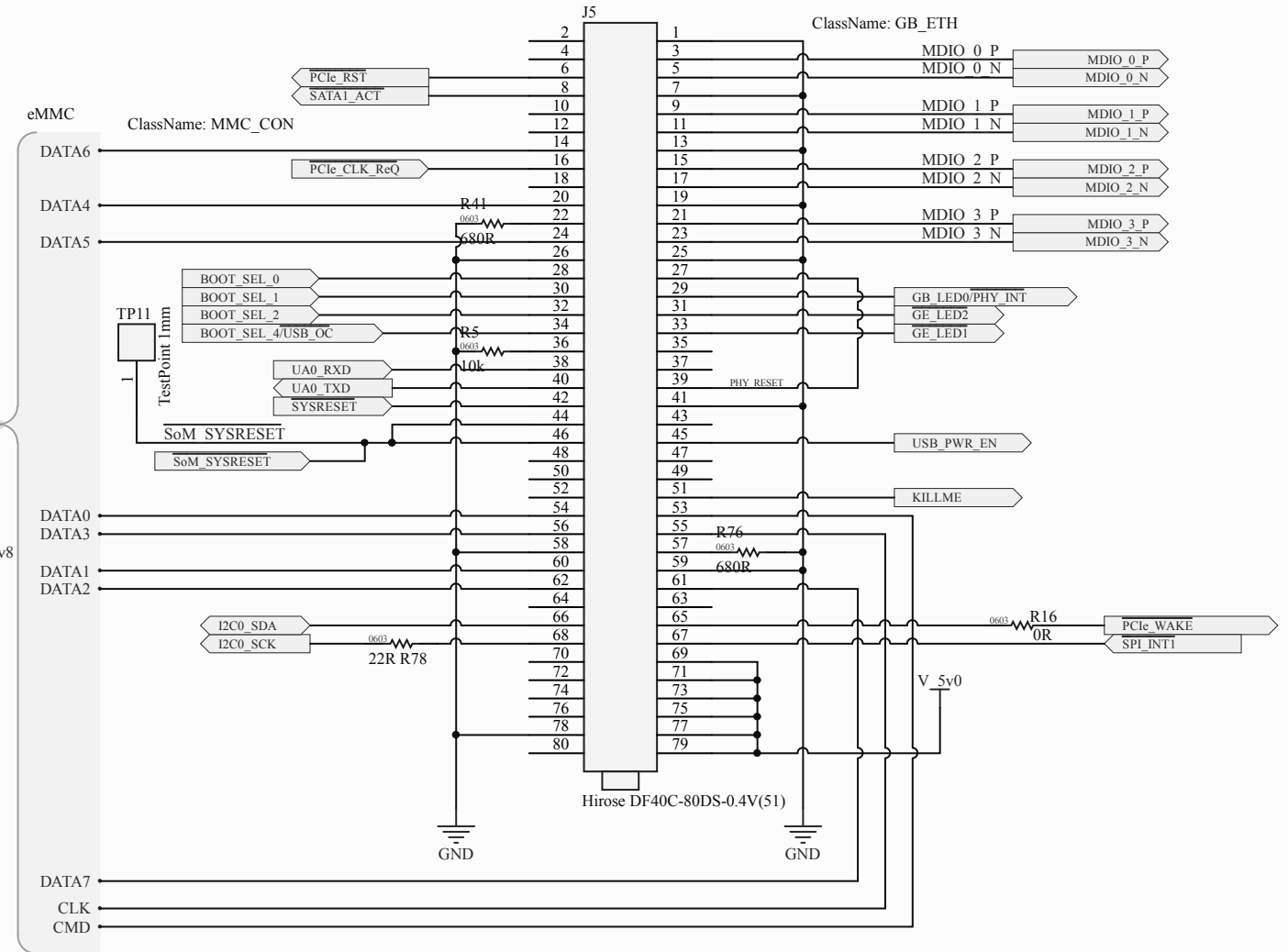
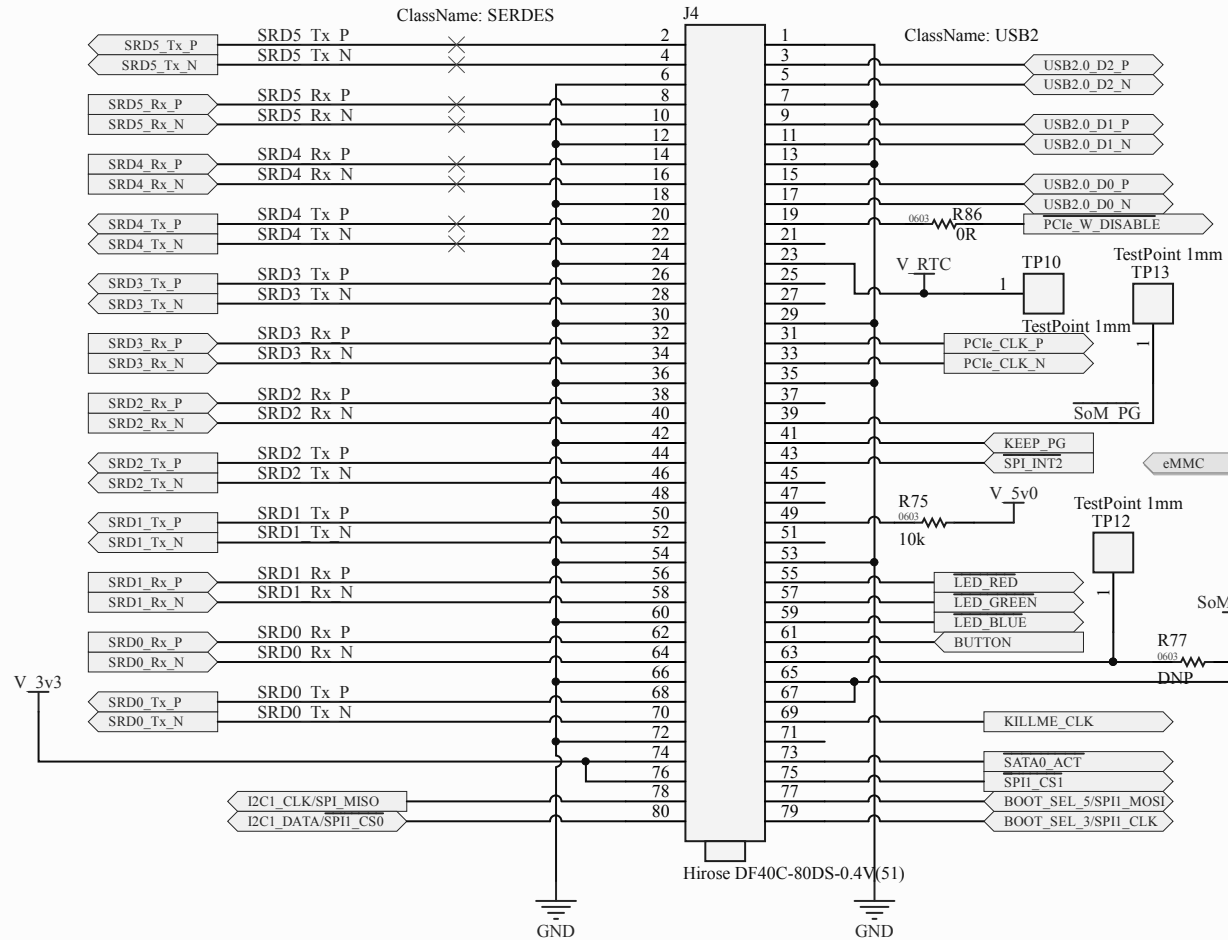
Title KEEP Base		OpenProducts Barsebäcksvägen 27 246 30 Löddeköpinge Sweden 556855-1344	
Size: A3	Revision: R1B	Sheet* of *	
Date: 2018-01-19	Time: 08:48:44		
File: Misc.SchDoc			

Parts not fitted (Comment set to 'DNP')



Title KEEP Base		OpenProducts Barsebäcksvägen 27 246 30 Löddeköpinge Sweden	
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Date: 2018-01-19	Time: 08:48:44	Sheet* of *	
File: PCIe.SchDoc			

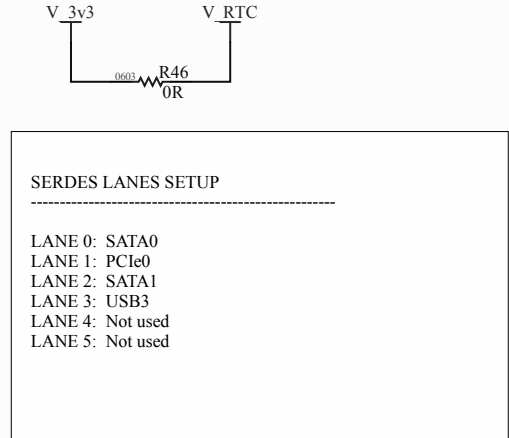




Pin Name	MPP setting	Fuction
MPP0	0x1	UART0 RX
MPP1	0x1	UART0 TX
MPP2	0x1	I2C SCK
MPP3	0x1	I2C SDA
MPP30	0x0	GPIO, PCIe_W_Disable (active low)
MPP34	0x0	GPIO, USB_PE (active low output)
MPP41	0x0	GPIO, KILLME
MPP42	0x0	GPIO, USB_OC (active low input)
MPP43	0x2	PCIe0_CLKREQ (in)
MPP44	0x0	GPIO, PCIe_W_DISABLE (active low output)
MPP46	0x2	PCIe0_RSTOUTn (out)
MPP48	0x0	GPIO, LED RED
MPP49	0x0	GPIO, LED GREEN
MPP50	0x0	GPIO, LED BLUE
MPP51	0x0	GPIO, Button detect (active low)
MPP52	0x0	GPIO, KILLME_CLK
MPP53	0x1	SATA1 Activity
MPP54	0x1	SATA0 Activity
MPP55	0x0	GPIO, (0x4 =>SPI1_CSn[1])
MPP56	0x0	GPIO, (0x4 =>SPI1_MOSI)
MPP57	0x0	GPIO, (0x4 =>SPI1_CLK)
MPP58	0x2	I2C1_SCK (in/out), (0x4 =>SPI1_MISO)
MPP59	0x2	I2C1_SDA (in/out), (0x4 =>SPI1_CS0)

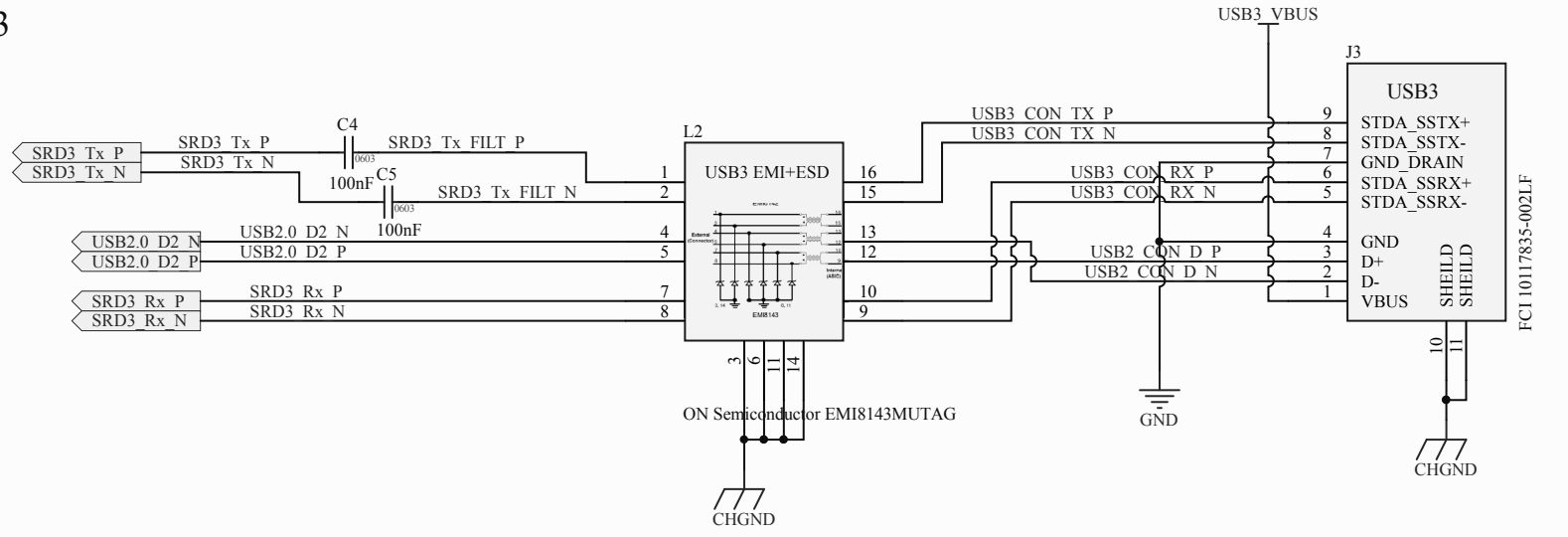
MPP[24]-MPP[27] are set up by reset to SDIO controller and should not be altered by SW
(These is used for other purposes by the Clearfog board)

MPP[56]-MPP[59] can be configured by hw during reset for SPI1 operation, see boot config

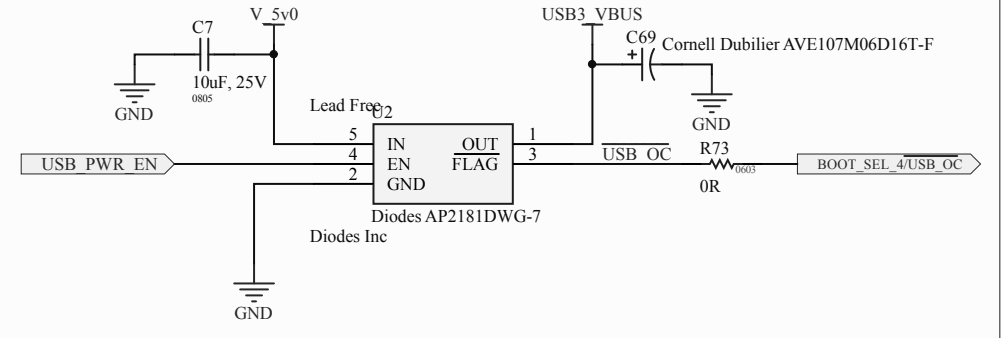


SoM1
A388 MicroSoM
Solid-Run MicroSoM A388

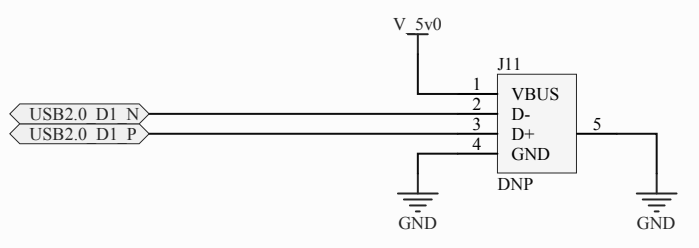
USB3

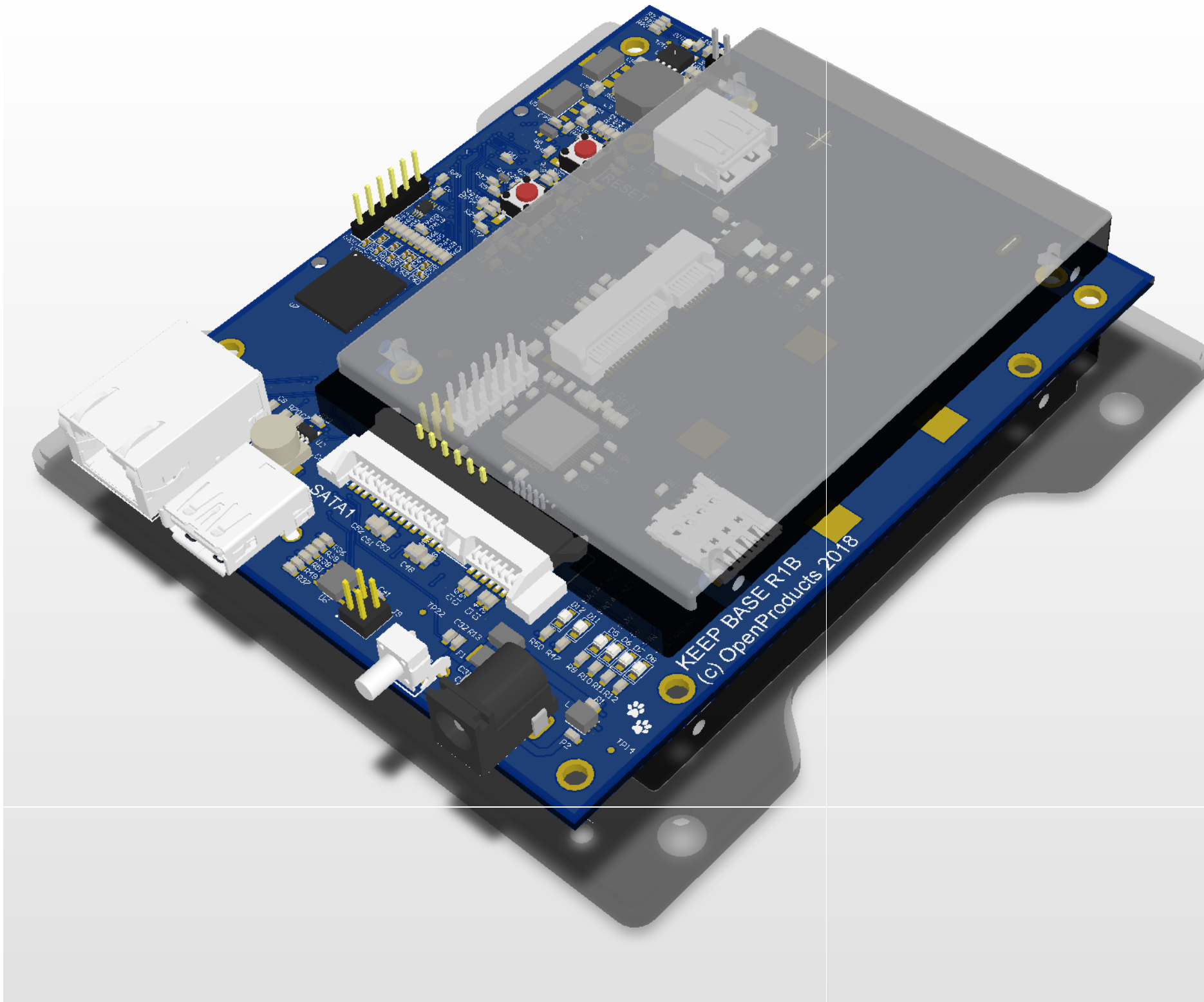


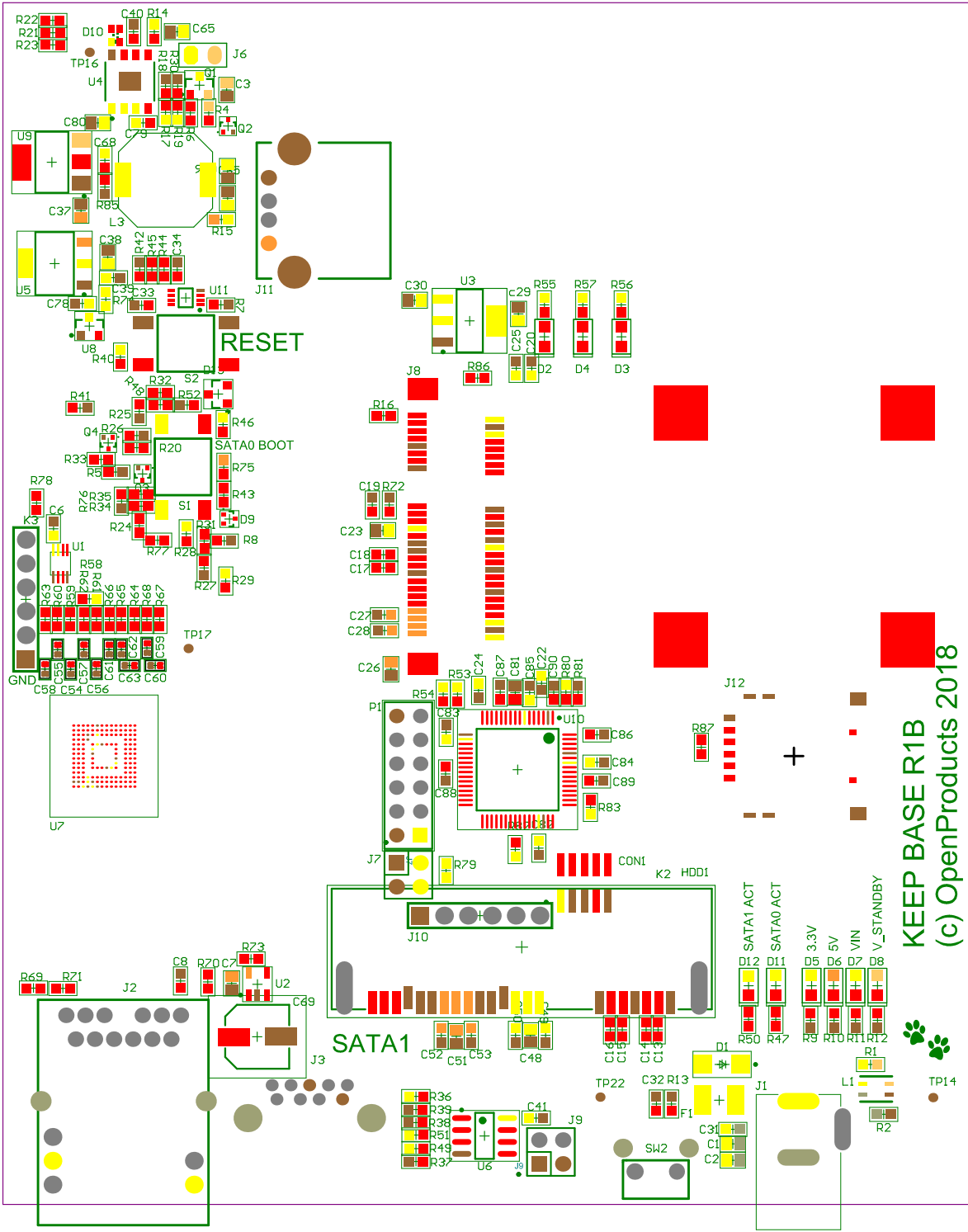
USB Power Enable / Supervision



Internal USB2.0 port







KEEP BASE R1B
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