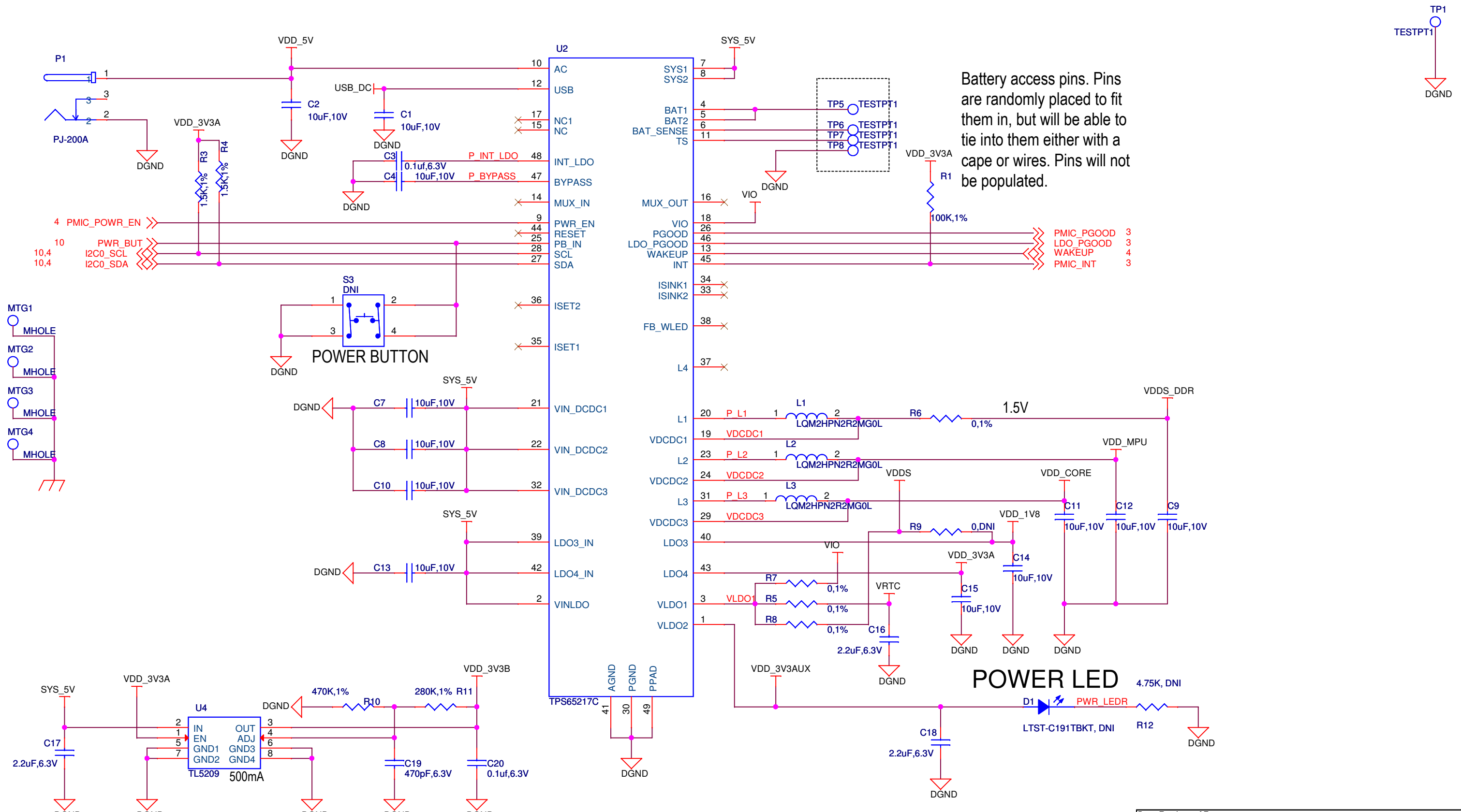


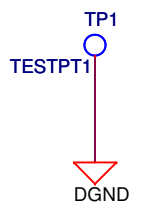
REV	Description	DATE	BY
A	Initial production Release. (based on BBB Rev A6)	11/15/2013	CCO
B	Initial production Release. (based on BBB Rev A6)	03/12/2014	CCO


PAGE NO.	SCHEMATIC PAGE
1	COVER PAGE
2	POWER MANAGEMENT
3	PROCESSOR 1 OF 3, JTAG HEADER
4	PROCESSOR 2 OF 3, UAB PORTS
5	PROCESSOR 3 OF 3
6	LED, CONFIGURATION AND BUTTON
7	DDR3 MEMORY
8	eMMC FLASH
9	10/100 ETHERNET
10	EXP CONN, uSD

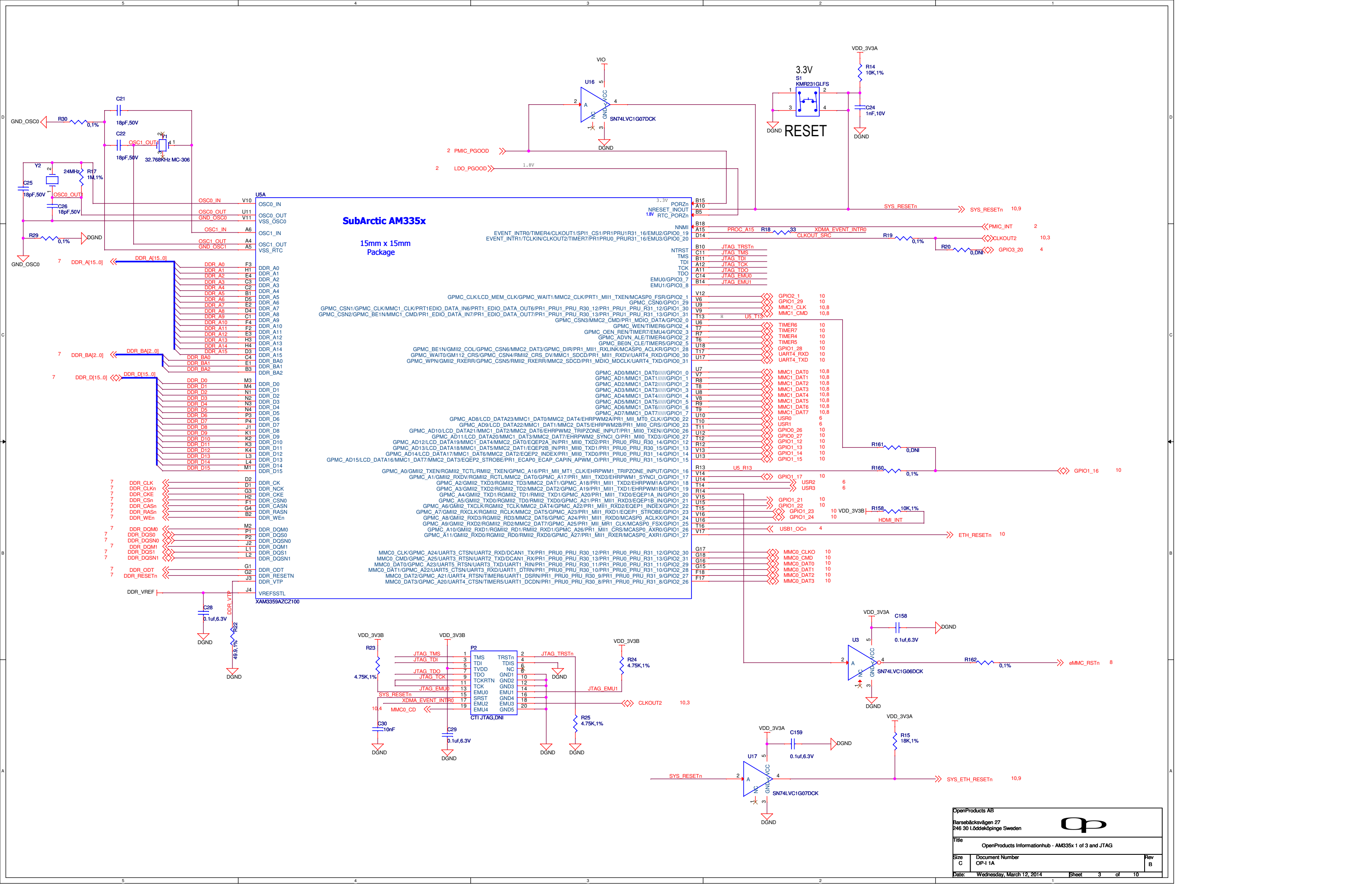
NOTE: PCB Revision for this board is Rev A



Battery access pins. Pins are randomly placed to fit them in, but will be able to tie into them either with a cape or wires. Pins will not be populated.



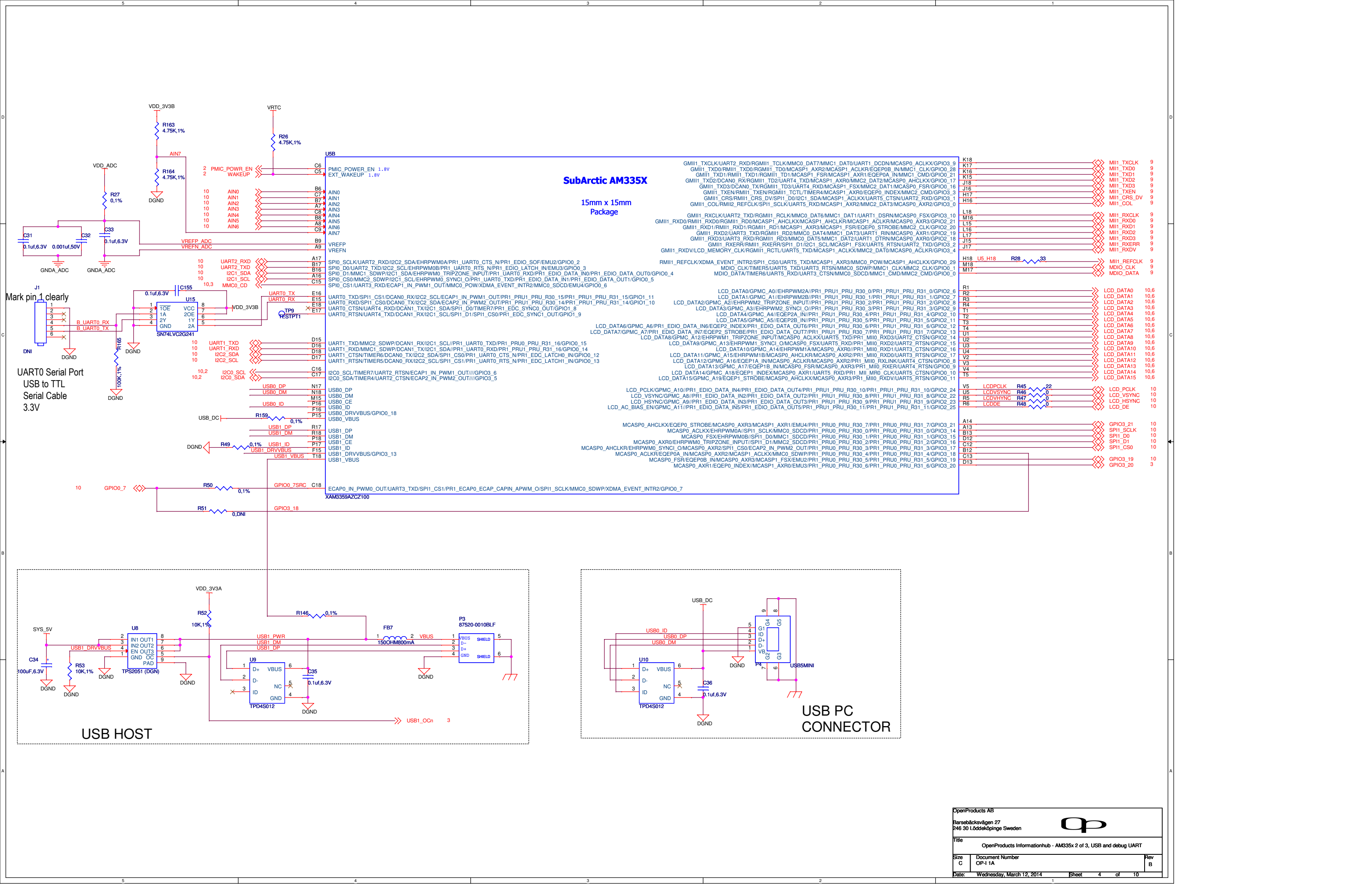
OpenProducts AB		
Barsebäcksvägen 27 246 30 Löddeköpinge Sweden		
		
Title OpenProducts Informationhub - PMIC		
Size B	Document Number OP-I 1A	Rev B
Date: Wednesday, March 12, 2014	Sheet 2	of 10

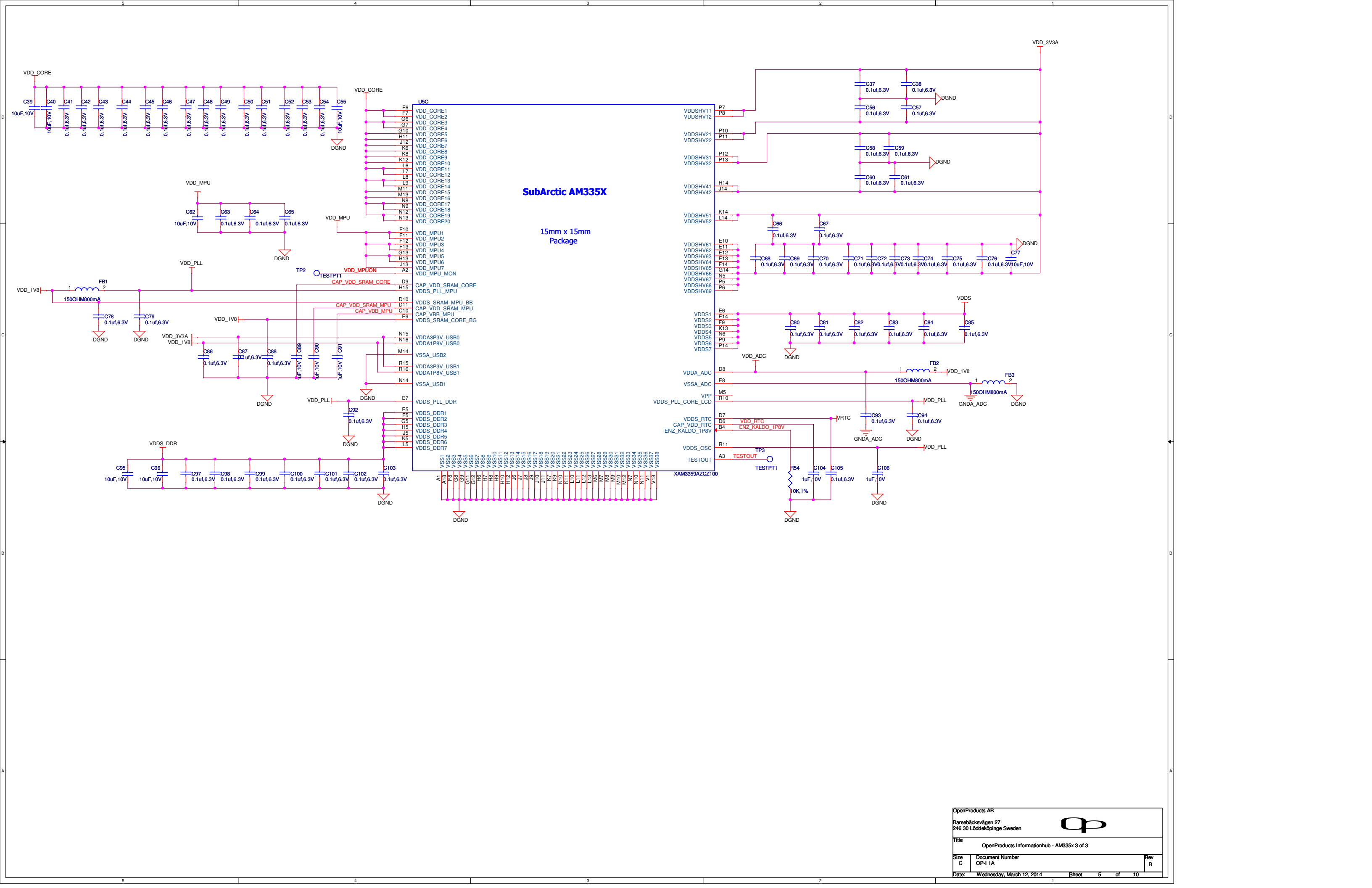


SubArctic AM335x

15mm x 15mm Package

USA	OSC0_IN	V10	OSC0_IN	B15	3.3V PORZn	B15	PROC_A15	R18	33	XDMA_EVENT_INTR0	10.9	SYS_RESETrn	10.9
	OSC0_OUT	U11	OSC0_OUT	A10	NRESET_INOUT	B5	CLKOUT_SRC	R19	0.1%	CLKOUT2	10.3	PMIC_INT	2
	VSS_OSC0	V11	VSS_OSC0	B5	RTC_PORZn					GPIO3_20	4		
	OSC1_IN	A6	OSC1_IN	B18	NNMI								
	OSC1_OUT	A4	OSC1_OUT	D14	EVENT_INTR0/TIMER4/CLKOUT1/SP1_CS1/PR1_PRU1R31_16/EMU2/GPIO0_19								
	VSS_RTC	A5	VSS_RTC	A15	EVENT_INTR1/TCLKIN/CLKOUT2/TIMER7/PR1_PRU0_PPRUR31_18/EMU3/GPIO0_20								
	DDR_A[15.0]	F3	DDR_A0	B10	JTAG_TRSTn								
	DDR_A1	H1	DDR_A1	C11	JTAG_TMS								
	DDR_A2	E4	DDR_A2	B11	JTAG_TDI								
	DDR_A3	C3	DDR_A3	A12	JTAG_TCK								
	DDR_A4	C2	DDR_A4	A11	JTAG_TDO								
	DDR_A5	B1	DDR_A5	C14	JTAG_EMU0								
	DDR_A6	D5	DDR_A6	B14	JTAG_EMU1								
	DDR_A7	E2	DDR_A7	V12	GPIO2_1	10							
	DDR_A8	D4	DDR_A8	V6	GPIO2_29	10							
	DDR_A9	C1	DDR_A9	U9	MMC1_CLK	10.8							
	DDR_A10	F4	DDR_A10	V9	MMC1_CMD	10.8							
	DDR_A11	F2	DDR_A11	T13	MMC1_DATA4	10.8							
	DDR_A12	E3	DDR_A12	U6	TIMER6	10							
	DDR_A13	H3	DDR_A13	T7	TIMER7	10							
	DDR_A14	H4	DDR_A14	R7	TIMER4	10							
	DDR_A15	E1	DDR_A15	T6	TIMER5	10							
	DDR_BA0	C4	DDR_BA0	U8	GPIO1_28	10							
	DDR_BA1	E1	DDR_BA1	T17	GPIO1_28	10							
	DDR_BA2	B3	DDR_BA2	U17	UART4_RXD	10							
	DDR_D0	M3	DDR_D0	U7	UART4_TXD	10							
	DDR_D1	M4	DDR_D1	V7	MMC1_DAT0	10.8							
	DDR_D2	N1	DDR_D2	R8	MMC1_DAT1	10.8							
	DDR_D3	N2	DDR_D3	T8	MMC1_DAT2	10.8							
	DDR_D4	N3	DDR_D4	U8	MMC1_DAT3	10.8							
	DDR_D5	N4	DDR_D5	V8	MMC1_DAT4	10.8							
	DDR_D6	P3	DDR_D6	R9	MMC1_DAT5	10.8							
	DDR_D7	P4	DDR_D7	T9	MMC1_DAT6	10.8							
	DDR_D8	J1	DDR_D8	U10	MMC1_DAT7	10.8							
	DDR_D9	K1	DDR_D9	T10	USR0	6							
	DDR_D10	K2	DDR_D10	T11	USR1	6							
	DDR_D11	K3	DDR_D11	U12	GPIO0_26	10							
	DDR_D12	K4	DDR_D12	U12	GPIO0_27	10							
	DDR_D13	L3	DDR_D13	T12	GPIO1_12	10							
	DDR_D14	L4	DDR_D14	R12	GPIO1_12	10							
	DDR_D15	M1	DDR_D15	V13	GPIO1_13	10							
	DDR_CLK	D1	DDR_CLK	U13	GPIO1_14	10							
	DDR_CLKn	G3	DDR_CLKn	R13	GPIO1_17	10							
	DDR_CKE	H2	DDR_CKE	U14	GPIO1_17	10							
	DDR_CS0n	F1	DDR_CS0n	U14	USR2	6							
	DDR_CAS0n	G4	DDR_CAS0n	T14	USR3	6							
	DDR_RAS0n	B2	DDR_RAS0n	R14	GPIO1_19	10							
	DDR_WE0n	B2	DDR_WE0n	G17	GPIO1_21	10							
	DDR_DQM0	M2	DDR_DQM0	U15	GPIO1_22	10							
	DDR_DQS0	P1	DDR_DQS0	T15	GPIO1_22	10							
	DDR_DQS0n	L2	DDR_DQS0n	V15	GPIO1_23	10							
	DDR_DQM1	J2	DDR_DQM1	U16	GPIO1_24	10							
	DDR_DQS1	L2	DDR_DQS1	T16	GPIO1_24	10							
	DDR_DQS1n	J3	DDR_DQS1n	U16	GPIO1_24	10							
	DDR_ODT	G1	DDR_ODT	T16	USB1_OCn	4							
	DDR_RESETrn	G2	DDR_RESETrn	V17	ETH_RESETrn	10							
	DDR_VTP	J4	DDR_VTP										
	VREFSSTL	J4	VREFSSTL										

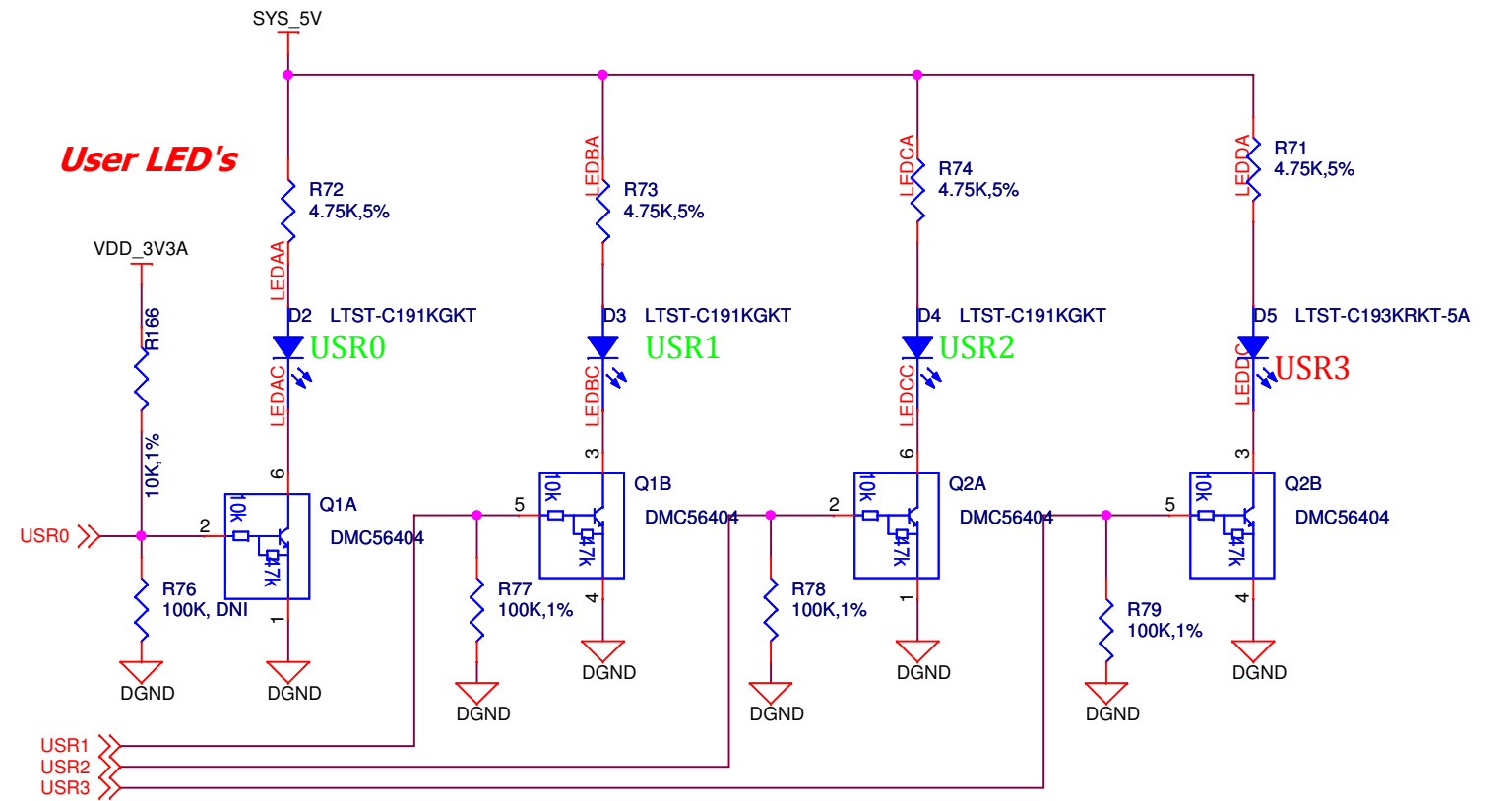
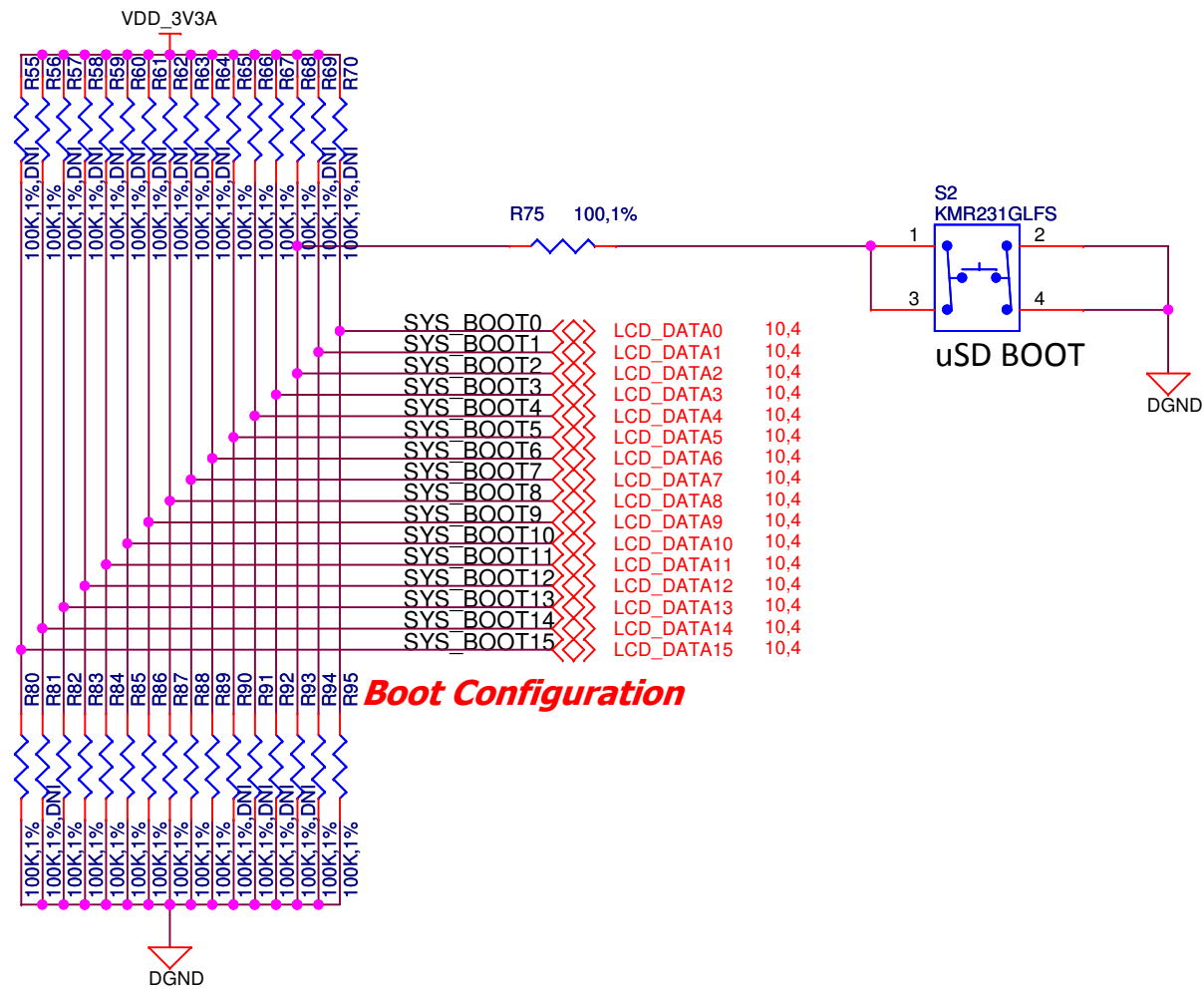




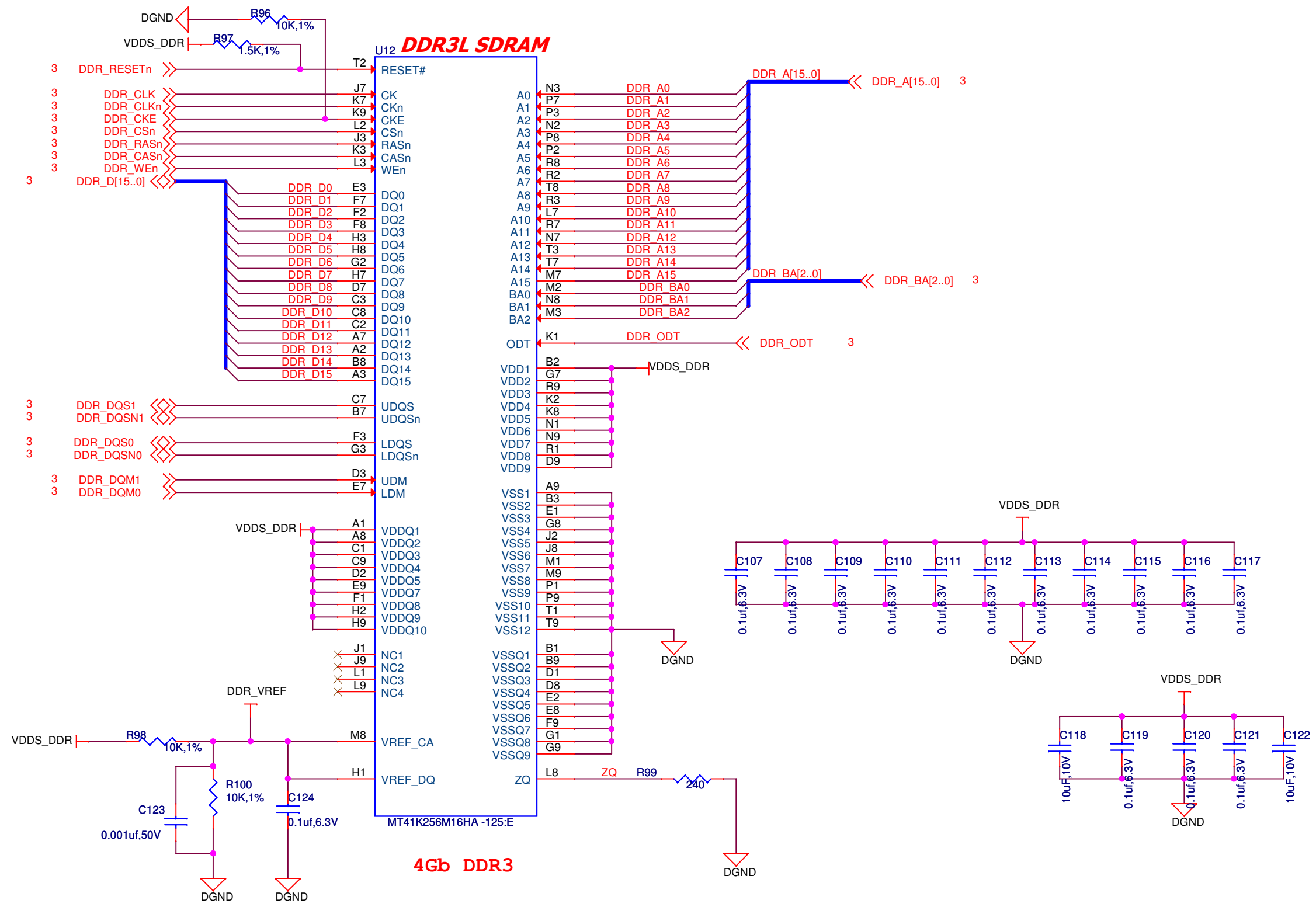
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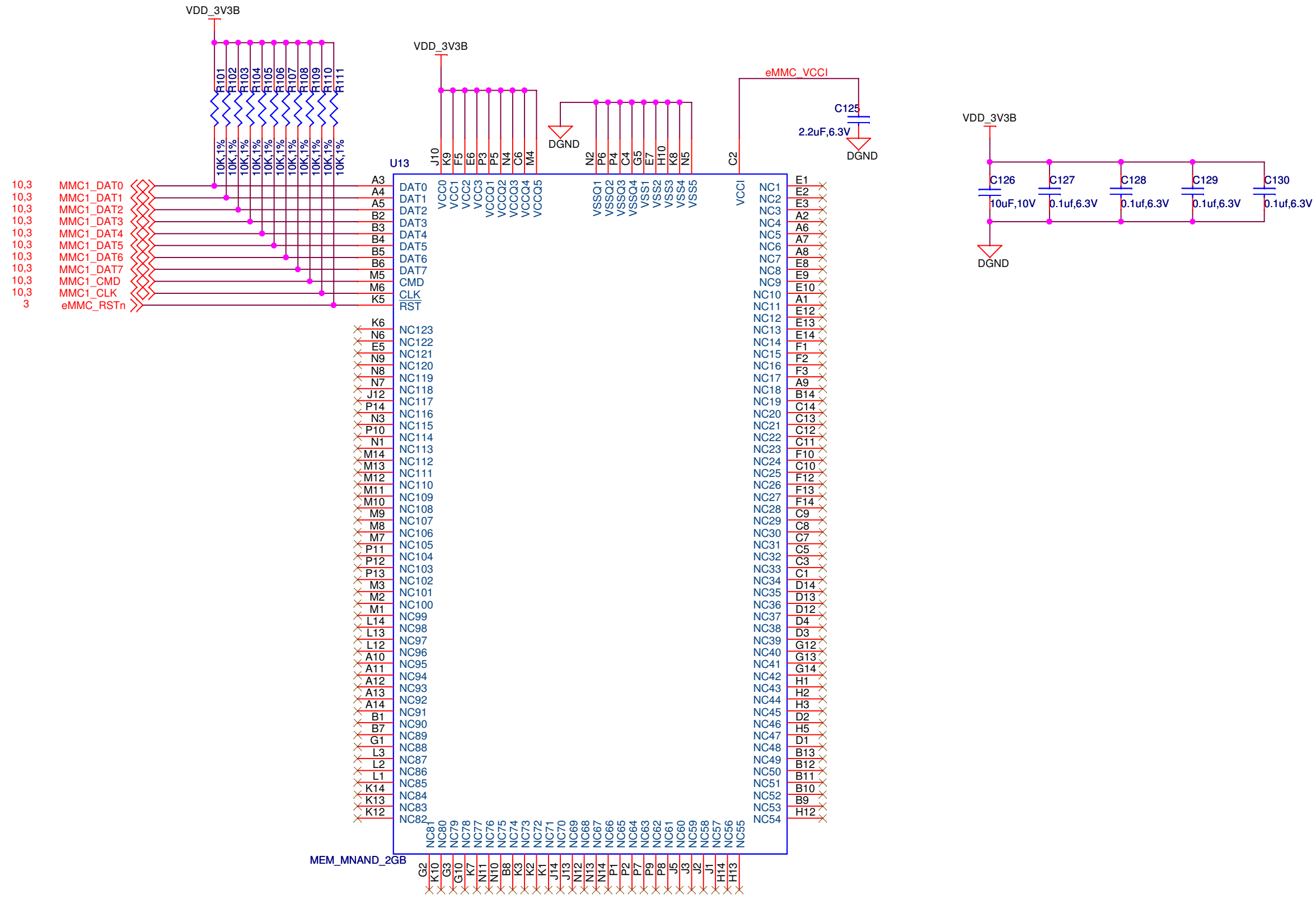
15mm x 15mm
Package

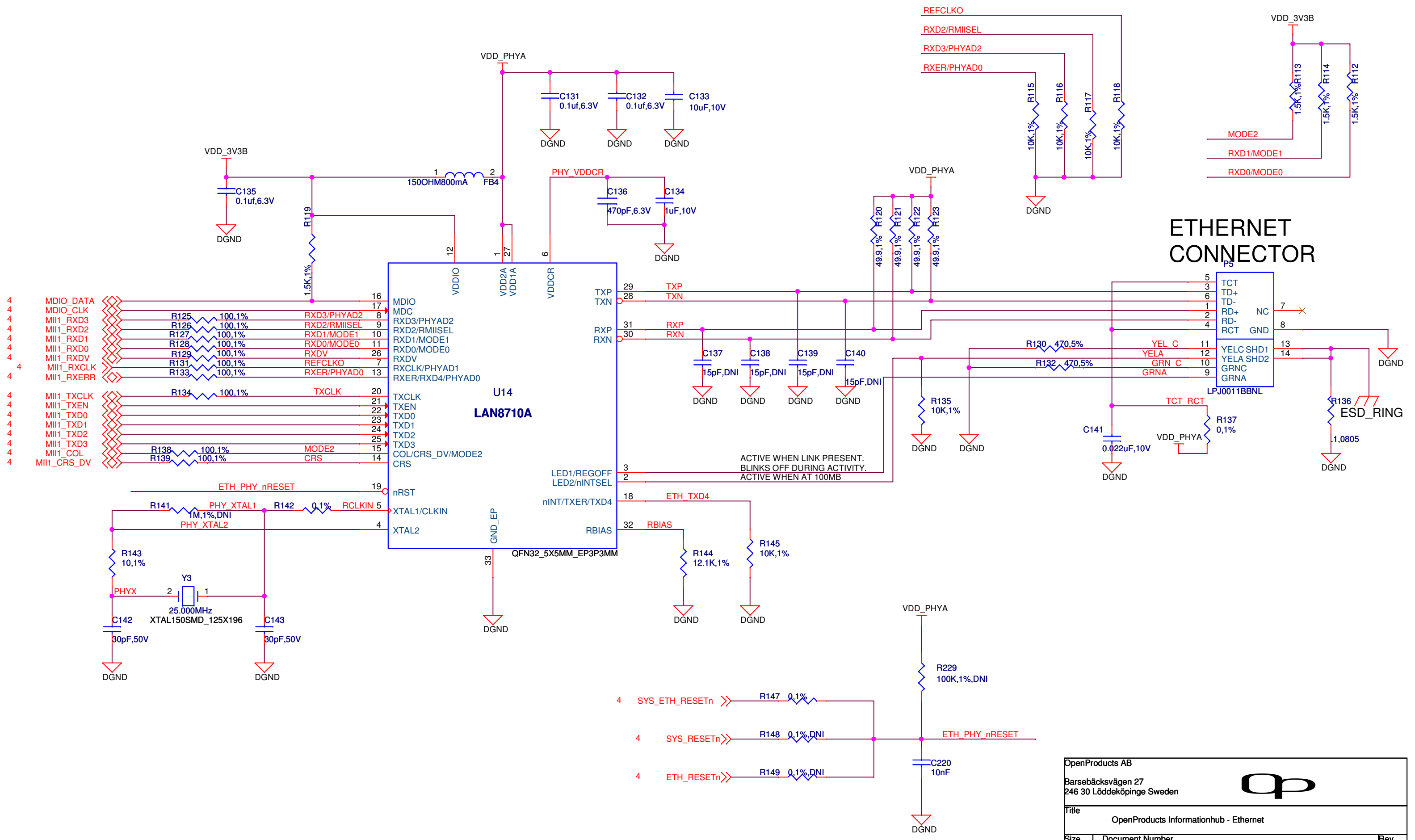
XAM3359AZC100




SYSBOOT[15:14]	SYSBOOT[13:12]	SYSBOOT[11:10]	SYSBOOT[9]	SYSBOOT[8]	SYSBOOT[7:6]	SYSBOOT[5]	SYSBOOT[4:0]	Boot Sequence			
00b = 19.2MHz 01b = 24MHz 10b = 25MHz 11b = 26MHz	00b (all other values reserved)	Don't care for ROM code	Don't care for ROM code	Don't care for ROM code	Don't care for ROM code	0 = CLKOUT1 disabled 1 = CLKOUT1 enabled	11100b	MMC1	MMC0	UART0	USB0[5]
00b = 19.2MHz 01b = 24MHz 10b = 25MHz 11b = 26MHz	00b (all other values reserved)	Don't care for ROM code	Don't care for ROM code	Don't care for ROM code	Don't care for ROM code	0 = CLKOUT1 disabled 1 = CLKOUT1 enabled	11000b	SPI0	MMC0	USB0[5] 1	UART0







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